CLAIMS

What is claimed is:

1. A system comprising:

a first integrated circuit (IC);

an interface coupled to the first IC; and

a second IC coupled to the interface, wherein the first IC simultaneously transmits the state of each of a plurality of signals not associated with the interface to the second IC in-band via the interface each time that a change in the state of one of the plurality of signals is detected.

2. The system of claim 1 wherein the state of all of the plurality of signals is sampled at the first IC whenever any of the signals change.

3. The system of claim 1 wherein the second IC drives each of the signals with new values received in-band each time that the plurality of signal values are received.

4. The system of claim 1 wherein the first IC comprises:

signal logic associated with each of the plurality of signals; and

protocol logic, coupled to the signal logic associated with each of the signals, to transmit the signal values in-band to the protocol to the second IC.

5. The system of claim 4 wherein the signal logic includes:

a first flip-flop with an input coupled to an associated signal and an

output coupled to the protocol logic, the output of the first flip-flop generating a held signal value; and

a second flip-flop having an input coupled to the output of the first flip-flop to receive the held signal value, the output of the second flip-flop generating a send signal.

6. The system of claim 4 wherein the signal logic includes:

a flip-flop with an input coupled to an associated signal and an output coupled to the protocol logic, the output of the flip-flop generating a held signal value; and

a counter having an input coupled to the output of the flip-flop to receive the held signal value, the output of the second flip-flop generating a send signal.

7. The system of claim 4 wherein the protocol logic selects a protocol point including all of the held signal values simultaneously and integrates the protocol point into a protocol that is transmitted to the second IC via the interface.

8. The system of claim 7 wherein the protocol point being transmitted is changed each time an additional signal transitions so that subsequent signal transitions are communicated with a short a latency.

9. The system of claim 1 wherein signal transitions that occur to close to previous transitions to be repeated between the first IC and the second IC via the

interface are discarded and more widely spaced transitions and the steady-state value of the signals is repeated.

10. The system of claim 1 wherein the second IC comprises:

protocol logic, coupled to the interface, to receive each of the in-band signals and to extract the state of each of the in-band signals; and

sequential logic, coupled to the protocol logic, to maintain the state of each of the in-band signals once the state has been received.

11. A method comprising:

monitoring the state of each of a plurality of signals at a first integrated circuit (IC); and

transmitting the state of each of the plurality of signals in-band across an interface to a second IC each time that a change in the state of one of the plurality of signals is detected.

12. The method of claim 11 wherein monitoring the state of each of a plurality of signals at the first IC comprises:

monitoring a signal held value at protocol logic associated with each of the plurality of signals; and

monitoring a send signal at the protocol logic associated with all of the plurality of signals.

13. The method of claim 12 further comprising:

selecting a protocol point including all of the held values of the input signals simultaneously at the protocol logic: and

integrating the protocol point into a protocol that is transmitted to the second IC via the interface.

14. The method of claim 13 further comprising:

receiving the protocol point at the second IC; and

extracting the state of each of the plurality of in-band signals.

15. A system comprising:

a chipset;

an interface coupled to the chipset; and

an integrated circuit (IC) coupled to the chipset, wherein the chipset simultaneously transmits the state of each of a plurality of signals not associated with the interface to the IC in-band via the interface each time that a change in the state of one of the plurality of signals is detected.

16. The system of claim 15 wherein the state of all of the plurality of signals is sampled at the chipset whenever any of the signals change.

17. The system of claim 15 wherein the IC drives each of the signals with new values received in-band each time that the plurality of signal values are received.

18. The system of claim 15 wherein the chipset comprises:

signal logic associated with each of the plurality of signals; and

protocol logic, coupled to the signal logic associated with each of the signals, to transmit the signal values in-band to the protocol to the IC.

19. The system of claim 18 wherein the signal logic includes:

a first flip-flop with an input coupled to an associated signal and an output coupled to the protocol logic, the output of the first flip-flop generating a held signal value; and

a second flip-flop having an input coupled to the output of the first flip-flop to receive the held signal value, the output of the second flip-flop generating a send signal.

20. The system of claim 18 wherein the signal logic includes:

a flip-flop with an input coupled to an associated signal and an output coupled to the protocol logic, the output of the flip-flop generating a held signal value; and

a counter having an input coupled to the output of the flip-flop to receive the held signal value, the output of the counter generating a send signal.

21. The system of claim 18 wherein the protocol logic selects a protocol point including all of the held signal values simultaneously and integrates the protocol

point into a protocol that is transmitted to the IC via the interface.

22. The system of claim 21 wherein the protocol point being transmitted is changed each time a held signal transitions so that subsequent signal transitions are communicated with a short a latency.

23. The system of claim 15 wherein signal transitions that occur to close to previous transitions to be repeated between the chipset and the IC via the interface are discarded and more widely spaced transitions and the steady-state value of the signals is repeated.

24. The system of claim 15 wherein the IC comprises:

protocol logic, coupled to the interface, to receive each of the in-band signals and to extract the state of each of the in-band signals; and

sequential logic, coupled to the protocol logic, to maintain the state of each of the in-band signals once the state has been received.